Listing of the Claims

1. (original) A stacked integrated circuit (IC) MIM capacitor structure comprising:

a first MIM capacitor structure formed in a first IMD layer comprising a first upper and first lower electrode portions;

at least a second MIM capacitor structure arranged in stacked relationship in an overlying IMD layer comprising a second upper electrode and second lower electrode to form an MIM capacitor stack;

wherein, the first lower electrode is arranged in common electrical signal communication comprising metal filled vias with the second upper electrode and the first upper electrode is arranged in common electrical signal communication with the second lower electrode.

2. (original) The stacked MIM capacitor structure of claim 1, further comprising at least one additional MIM capacitor structure arranged in stacked relationship with respect to the at least a second MIM capacitor structure wherein respective upper and lower electrodes of respective odd and even numbered MIM capacitor structures in the MIM capacitor stack comprise a commonly communicating electrical interconnect structure in parallel electrical relationship.

3. (original) The stacked MIM capacitor structure of claim 1, wherein the upper electrodes including electrically communicating metal filled vias of the respective MIM structures in the MIM capacitor stack comprise a substantially identical structure.

4. (original) The stacked MIM capacitor structure of claim 1, wherein the lower electrodes including electrically communicating metal filled vias of the respective MIM structures in the MIM capacitor stack comprise a substantially identical structure in alternating IMD layers.

5. (original) The stacked MIM capacitor structure of claim 1, further comprising a capacitor dielectric sandwiched between the respective upper and lower electrodes selected from the group consisting of SiO_2, Si_3N_4, TiO_2, Ta_2O_5, ZrO_2, Y_2O_3, La_2O_5, and HfO_2.

6. (original) The stacked MIM capacitor structure of claim 1, wherein the metal filled vias comprise a metal selected from the group consisting of Al, Cu, W, and alloys thereof.

7. (original) The stacked MIM capacitor structure of claim 1, wherein the metal filled vias comprise a metal selected from the group consisting essentially of W.

8. (original) The stacked MIM capacitor structure of claim 1, wherein the respective upper and lower electrodes comprise a metal selected from the group consisting of Al, Cu, Ta, Ti, and nitrides thereof.

9. (original) The stacked MIM capacitor structure of claim 8, wherein the nitrides thereof comprise silicided nitrides.

10. (original) The stacked MIM capacitor structure of claim 1, further comprising bonding pads formed in electric signal communication with the uppermost MIM capacitor structure.

11. (original) The stacked MIM capacitor structure of claim 1, wherein the lowermost MIM capacitor structure is formed in an IMD layer greater than about a second IMD layer formed over the semiconductor wafer.

12. (withdrawn) A method of forming a stacked MIM capacitor integrated circuit (IC) structure comprising the steps of:

a) providing a multilayer semiconductor device comprising at least one underlying IMD layer;

b) forming first MIM capacitor structure comprising a first upper and first lower electrode portions sandwiching a first capacitor dielectric;

c) blanket depositing a first IMD layer over the first capacitor structure;

d) forming at least one first metal filled via interconnect in electrical communication with the first lower electrode and at least one second metal filled via interconnect in electrical communication with the first upper electrode;

e) forming a second MIM capacitor structure arranged in stacked relationship overlying the first MIM capacitor structure comprising a second upper and second lower electrode portions sandwiching a second capacitor dielectric said second lower electrode portion formed in electrical communication with the at least one second metal filled via interconnect;

f) blanket depositing a second IMD layer over the second IMD structure;

g) forming at least one third metal filled via interconnect in electrical communication with the second lower electrode; at least one fourth metal filled via formed in stacked relationship and electrical communication with the at least one first metal filled via; and, at least one fifth metal filled via in electrical communication with the second upper electrode; and,

h) providing a first metal bonding pad in electrical communication with the at least one fourth and at least one fifth metal filled vias and a second metal bonding pad in electrical communication with the at least one third metal filled via to form a stacked MIM capacitor structures in equivalent circuit parallel relationship.

13. (withdrawn) The method of claim 1 wherein steps b) through d) are repeated to form a third MIM capacitor structure comprising a lower electrode in electrical communication with the first MIM capacitor structure lower electrode and an upper electrode in electrical communication with the first MIM capacitor structure upper electrode.

14. (withdrawn) The method of claim 12, wherein steps b) through g) are repeated to form odd numbered MIM capacitor structures and even numbered MIM capacitor structures in common electrical communication.

15. (withdrawn) The method of claim 12, wherein the respective upper electrodes are formed according to a photolithographic patterning and etching process using a common mask.

16. (withdrawn) The method of claim 12, wherein the respective upper and lower electrodes are formed according to the steps:

blanket depositing at least one lower conductive layer comprising a metal;

blanket depositing a capacitor dielectric layer;

blanket depositing at least one upper conductive layer comprising a metal;

photolithographically patterning and RIE etching to form the upper electrode and capacitor dielectric; and,

photolithographically patterning and RIE etching to define the lower electrode having a larger width compared to the lower electrode.

17. (withdrawn) The method of claim 12, wherein the capacitor dielectric is selected from the group consisting of SiO_2, Si_3N_4, TiO_2, Ta_2O_5, ZrO_2, Y_2O_3, La_2O_5, and HfO_2.

18. (withdrawn) The method of claim 12, wherein the metal filled vias comprise a metal selected from the group consisting of Al, Cu, W, and alloys thereof.

19. (withdrawn) The method of claim 12, wherein the metal filled vias comprise a metal selected from the group consisting essentially of W.

20. (withdrawn) The method of claim 12, wherein the respective upper and lower electrodes comprise a metal selected from the group consisting of Al, Cu, Ta, Ti, and nitrides thereof.

21. (withdrawn) The method of claim 20, wherein the nitrides thereof comprise silicided nitrides.